S905

Quick Reference Manual

Revision: 0.6

Amlogic, Inc.

REVISION HISTORY

Revision Number	Revision Date	Changes
0.3	2015/3/26	Initial version release
0.4	2015/4/9	Correct VDD18_XTAL_CLK pin name and update operation conditions
0.5	2015/5/25	Update power on sequence and add analog unused pin connections
0.6	2015/6/18	Update video decoding capability

CONTACT INFORMATION

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Contents

1. General Description

S905 is an advanced application processor designed for OTT/IP Set Top Box(STB), smart projector and high-end media box applications. It integrates a powerful CPU/GPU subsystem, and a secured UHD video CODEC engine with all major peripherals to form the ultimate low power multimedia AP.

The main system CPU is a quad-core ARM Cortex-A53 CPU with 32KB L1 instruction and 32KB data cache for each core and a large 512KB L2 unified cache to improve system performance. In addition, the Cortex-A53 CPU includes the NEON SIMD co-processor to improve software media processing capability. The quad-core ARM Cortex-A53 CPU can be overdriven to 2.0GHz and has a wide bus connecting to the memory sub-system.

The graphic subsystem consists of two graphic engines and a flexible video/graphic output pipeline. The five core ARM Mali-450 GPU including dual geometry processors (GP) and triple pixel processors (PP) handles all OpenGL ES 1.1/2.0 and OpenVG graphics programs, while the 2.5D graphics processor handles additional scaling, alpha, rotation and color space conversion operations. The video output pipeline can perform advanced video post-processing and enhancements. Together, the CPU and GPU handle all operating system, networking, user-interface and gaming related tasks.

Amlogic Video Engine (AVE) offloads the CPU by handling all video CODEC processing. It includes dedicated hardware video decoder and encoder. AVE is capable of decoding 4K2K resolution video at 60fps with complete Trusted Video Path (TVP) for secure applications and supports full formats including MVC, MPEG-1/2/4, VC-1/WMV, AVS, AVS+, RealVideo, MJPEG streams, H.264, H265-10 and also JPEG pictures with no size limitation. The independent encoder is able to encode in JPEG and H.264 up to 1080p at 60fps.

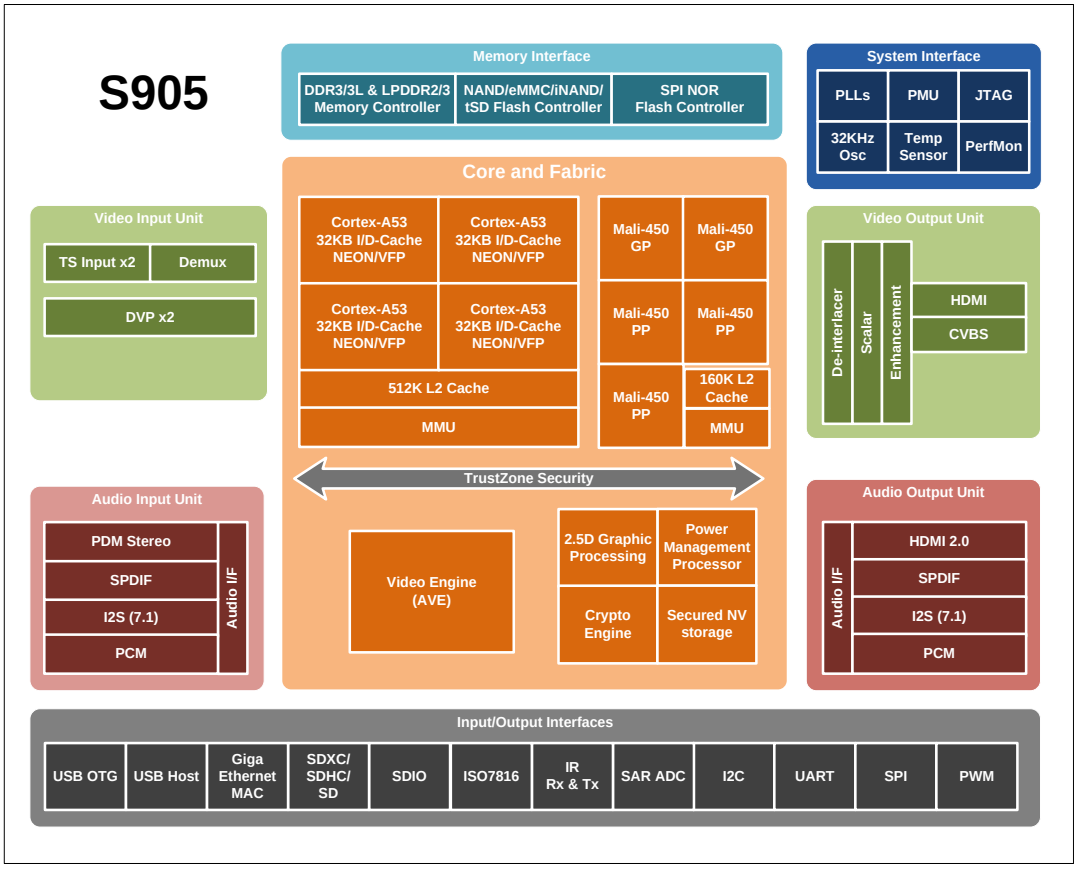
S905 integrates all standard audio/video input/output interfaces including a HDMI2.0 transmitter with 3D, CEC and HDCP 2.2 support, a CVBS output, I2S and SPDIF digital audio input/output interfaces, a PCM audio interface, two-channel PDM digital MIC inputs and dual DVP camera interfaces.

S905 also integrates a set of functional blocks for digital TV broadcasting streams. The built-in two demux can process the TV streams from the serial and parallel transport stream input interface, which can connect to external tuner/demodulator. An ISO7816 smart card interface and a crypto-processor are built in to help handling encrypted traffic and media streams.

The processor has rich advanced network and peripheral interfaces, including a Gigabit Ethernet MAC with RMII/RGMII interface, dual USB 2.0 high-speed ports (one OTG and one HOST) and multiple SDIO/SD card controllers, UART, I2C, high-speed SPI and PWMs.

Standard development environment utilizing GNU/GCC Android tool chain is supported. Please contact your AMLOGIC sales representative for more information.

2. Features Summary



CPU Sub-system

- Quad core ARM Cortex-A53 CPU up to 2.0GHz (DVFS)
- ARMv8-A architecture with Neon and Crypto extensions
- 8-stage in-order full dual issue pipeline
- 32KB instruction cache and 32KB data cache
- 512KB Unified L2 cache
- Advanced TrustZone security system
- Application based traffic optimization using internal QoS-based switching fabrics

3D Graphics Processing Unit

- Penta-core ARM Mali-450 GPU up to 750MHz+ (DVFS)
- Dual Geometry Processors with 32KB L2 cache
- Triple Pixel Processors with 128KB L2 caches
- Concurrent multi-core processing
- 2250Mpix/sec and 165Mtri/sec
- Full scene over-sampled 4X anti-aliasing engine with no additional bandwidth usage
- OpenGL ES 1.1/2.0 and OpenVG 1.1 support

2.5D Graphics Processor

- Fast bitblt engine with dual inputs and single output
- Programmable raster operations (ROP)
- Programmable polyphase scaling filter

- Supports multiple video formats 4:2:0, 4:2:2 and 4:4:4 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Fast color space conversion
- Advanced anti-flickering filter

Crypto Engine

- AES block cipher with 128/192/256 bits keys, standard 16 bytes block size and streaming ECB, CBC and CTR modes
- DES/TDES block cipher with ECB and CBC modes supporting 64 bits key for DES and 192 bits key for 3DES
- Hardware key-ladder operation and DVB-CSA for transport stream encryption
- Built-in hardware True Random Number Generator (TRNG), CRC and SHA-1/SHA-2 engine

Video/Picture CODEC

- Amlogic Video Engine (AVE) with dedicated hardware decoders and encoders
- Supports multiple "secured" video decoding sessions and simultaneous decoding and encoding
- Video/Picture Decoding
    - H.265 HEVC MP-10@L5.1 up to 4Kx2K@60fps
    - H.264 AVC HP@L5.1 up to 4Kx2K@30fps
    - H.264 MVC up to 1080p @60fps
    - MPEG-4 ASP@L5 up to 1080P@60fps (ISO-14496)
    - WMV/VC-1 SP/MP/AP up to 1080P@60fps
    - AVS-P16(AVS+) /AVS-P2 JiZhun Profile up to 1080P@60fps
    - MPEG-2 MP/HL up to 1080P@60fps (ISO-13818)
    - MPEG-1 MP/HL up to 1080P@60fps (ISO-11172)
    - RealVideo 8/9/10 up to 1080P
    - WebM up to VGA
    - Multiple language and multiple format sub-title video support
    - MJPEG and JPEG unlimited pixel resolution decoding (ISO/IEC-10918)
    - Supports JPEG thumbnail, scaling, rotation and transition effects
    - Supports *.mkv,*.wmv,*.mpg, *.mpeg, *.dat, *.avi, *.mov, *.iso, *.mp4, *.rm and *.jpg file formats
- Video/Picture Encoding
    - Independent JPEG and H.264 encoder with configurable performance/bit-rate
    - JPEG image encoding
    - H.264 video encoding up to 1080P@60fps with low latency
    - Video Post-Processing Engine
- Motion adaptive 3D noise reduction filter
- Advanced motion adaptive edge enhancing de-interlacing engine
- 3:2 pull-down support
- Programmable poly-phase scalar for both horizontal and vertical dimension for zoom and windowing
- Programmable color management filter (to enhance blue, green, red, face and other colors)
- Dynamic Non-Linear Luma filter
- Deblocking fliters
- Programmable color matrix pipeline
- Video mixer: 2 video planes and 2 graphics planes per video output

Video Output

- Built-in HDMI 2.0 transmitter including both controller and PHY with CEC and HDCP 2,2, 4Kx2K@60 max resolution output
- CVBS 480i/576i standard definition output
- Supports all standard SD/HD/FHD video output formats: 480i/p, 576i/p, 720p, 1080i/p and 4Kx2K

Camera Interface

- Two ITU 601/656 parallel video input with down-scalar
- Supports camera input as YUV422, RGB565,16bit RGB or JPEG

Audio Decoder and Input/Output

- Supports MP3, AAC, WMA, RM, FLAC, Ogg and programmable with 7.1/5.1 down-mixing
- I2S audio interface supporting 8-channel (7.1) input and output
- Built-in serial digital audio SPDIF/IEC958 output and PCM input/output
- Dual-channel digital microphone PDM input
- Supports concurrent dual audio stereo channel output with combination of I2S+PCM

Memory and Storage Interface

- 16/32-bit SDRAM memory interface running up to DDR2133
- Supports up to 2GB DDR3, DDR3L, LPDDR2, LPDDR3 with dual ranks
- Supports SLC/MLC/TLC NAND Flash with 60-bit ECC, compatible to Toshiba toggle mode in addition to ONFI 2.2
- SDSC/SDHC/SDXC card and SDIO interface with 1-bit and 4-bit data bus width supporting spec version 2.x/3.x/4.x DS/HS modes up to UHS-I SDR104
- eMMC and MMC card interface with 1/4/8-bit data bus width fully supporting spec version 5.0 HS400
- Supports serial 1, 2 or 4-bit NOR Flash via SPI interface
- Built-in 4k bits One-Time-Programming memory for key storage

Network

- Integrated IEEE 802.3 10/100/1000 Gigabit Ethernet controller with RMII/RGMII interface
- Supports Energy Efficiency Ethernet (EEE) mode
- Optional 50MHz and 125MHz clock output to Ethernet PHY
- WiFi/IEEE802.11 & Bluetooth supporting via SDIO/USB/UART/PCM
- Network interface optimized for mixed WIFI and BT traffic

Digital Television Interface

- Transport stream (TS) input interface with built-in demux processor for connecting to external digital TV tuner/demodulator
- Built-in PWM, I2C and SPI interfaces to control tuner and demodulator
- Integrated ISO 7816 smart card controller

Integrated I/O Controllers and Interfaces

- Dual USB 2.0 high-speed USB I/O, one USB Host and one USB OTG
- Multiple UART, I2C and SPI interface with slave select
- Multiple PWMs
- Programmable IR remote input/output controllers
- Built-in 10bit SAR ADC with 2 input channels
- A set of General Purpose IOs with built-in pull up and pull down

System, Peripherals and Misc. Interfaces

- Integrated general purpose timers, counters, DMA controllers
- 24 MHz crystal input and internal 32KHz oscillator
- Embedded debug interface using ICE/JTAG

Power Management

- Multiple external power domains controlled by PMIC
- Multiple internal power domains controlled by software
- Multiple sleep modes for CPU, system, DRAM, etc.
- Multiple internal PLLs for DVFS operation
- Multi-voltage I/O design for 1.8V and 3.3V
- Power management auxiliary processor in a dedicated always-on (AO) power domain that can communicate with an external PMIC

Security

- Trustzone based Trusted Execution Environment (TEE)
- Secured boot, encrypted OTP, internal control buses and storage
- Protected memory regions and electric fence data partition
- Hardware based Trusted Video Path (TVP) and secured contents (needs SecureOS software)

Package

- LFBGA,13x13mm, 19x19 ball matrix, 0.65 ball pitch, RoHS compliant